

WHAT IS CLAIMED IS:

1. A semiconductor apparatus comprising an analog generation circuit including a resistive element, a capacitive element and a switching element for generating a voltage determined by a conduction time of the switching element and by a time constant of the resistive and capacitive elements based on a current flowing through the resistive element controlled by turning ON and OFF of the switching element, wherein an output voltage of the analog generation circuit is transmitted to another circuit or element arranged on a semiconductor chip through a first transmission line, the voltage transmitted to the another circuit or element is fed back to the analog generation circuit through a second transmission line, and the analog generation circuit generates the output voltage according to the fed-back voltage.
2. A semiconductor apparatus as set forth in claim 1, wherein the analog generation circuit can generate an arbitrary voltage according to a pulse width of a signal for control of the switching element.
3. A semiconductor apparatus as set forth in claim 1, wherein the analog generation circuit is a test circuit for generating a voltage for inspection of the another circuit or element arranged on the semiconductor chip.
4. A semiconductor apparatus as set forth in claim 1, wherein the analog generation circuit is a

function circuit for taking a role of part of a function of the semiconductor apparatus.

5. A semiconductor apparatus as set forth in claim 1, wherein a plurality of the analog generation circuits are provided in a zone on the semiconductor chip other than zones for formation of circuit blocks, part of the analog generation circuits is formed as a repair circuit for repairing a defect portion present in any of the function circuits taking a role of part of the functions of the semiconductor apparatus.

6. A semiconductor apparatus wherein a variable logic cell and a variable analog cell are provided in a zone on a semiconductor chip other than block formation zones of original function circuits, the variable logic cell including:

a variable logic circuit having memory elements for outputting a logic output in response to an input according to memory information of the memory elements;

variable wiring means having switching elements for connecting and disconnecting a plurality of signal lines for connection of the variable logic circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means, the variable analog cell including:

an analog generation circuit having a resistive element and a capacitive element for generating a voltage determined by a conduction time of the switching elements and by a time constant of the resistive and capacitive elements based on a current flowing through the resistive element controlled by turning ON and OFF operation of the switching elements;

variable wiring means for connecting or disconnecting a plurality of signal lines for connection of the analog generation circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means.

7. A semiconductor apparatus as set forth in claim 6, wherein the variable wiring means and wiring-line connection state memory means in the variable logic and analog cells have identical structures respectively, and the variable logic circuit and the analog generation circuit are formed each by elements selected from an identical group of elements formed on the semiconductor chip.

8. A semiconductor apparatus as set forth in claim 6, wherein the analog generation circuit is arranged to generate a voltage according to a pulse width of a signal for control of the switching elements.

9. A semiconductor apparatus as set forth in claim 6, wherein a circuit for generating the signal for control of the switching elements is formed as the variable logic cell.

10. A semiconductor apparatus as set forth in claim 6, wherein the analog generation circuit forms a test circuit for generating a voltage for inspection of another circuit or element arranged on the semiconductor chip.

11. A semiconductor apparatus as set forth in claim 6, wherein the analog generation circuit is a function circuit for taking a role of part of functions of the semiconductor apparatus.

12. A semiconductor apparatus comprising four memory cells to be alternatively selected according to a combination of signals of positive and negative phases, wherein a variable logic cell and a variable analog cell are provided in a zone on a semiconductor chip other than block formation zones of original function circuits, the variable logic cell including:

a plurality of variable logic cells arranged to outputting signals of positive and negative phases according to memory data of the selected memory cell;

variable wiring means having switching elements for connecting or disconnecting a plurality of signal line pairs for connection of the variable logic circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means,

the variable analog cell including:
an analog generation circuit having a resistive element and a capacitive element for generating a voltage determined by a conduction time of the switching elements and by a time constant of the resistive and capacitive elements based on a current flowing through the resistive element controlled by turning ON and OFF operation of the switching elements;

variable wiring means having switching elements for connecting or disconnecting a plurality of signal line pairs for connection of the analog generation circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means, and
wherein the variable logic cell transmits a signal via the signal lines pairs in a differential system, and the variable analog cell outputs a voltage generated via one of the signal lines in pair and receives a feedback voltage via the other of the signal lines in pair.

13. A semiconductor apparatus as set forth in claim 12, wherein the analog generation circuit is arranged to generate a voltage according to a pulse

width of a signal for control of the switching elements.

14. A semiconductor apparatus as set forth in claim 12, wherein a circuit for generating the signal for control of the switching elements is formed as the variable logic cell.

15. A semiconductor apparatus as set forth in claim 12, wherein the analog generation circuit is formed as a test circuit for generating a voltage for inspection of another circuit or element arranged on the semiconductor chip.

16. A semiconductor apparatus as set forth in claim 12, wherein the analog generation circuit is formed as a function circuit for taking a role of part of functions of the semiconductor apparatus.

17. A semiconductor apparatus as set forth in claim 12, wherein a plurality of the analog generation circuits are provided in zones on the semiconductor chip other than zones for formation of circuit blocks, part of the analog generation circuits is formed as a repair circuit for repairing a defective part present in any of the function circuits taking a role of part of the functions of the semiconductor apparatus.

18. A semiconductor apparatus comprising an analog circuit, wherein an output voltage of the analog circuit is transmitted via a first transmission line to another circuit or element arranged on a semiconductor chip, the voltage transmitted to the another circuit or

element is fed back to the analog circuit via a second transmission line, and the analog circuit generates the output voltage according to the fed-back voltage.

19. A semiconductor apparatus as set forth in claim 18, wherein the analog circuit is a test circuit for generating a voltage for inspection of another circuit or element arranged on the semiconductor chip.

20. A semiconductor apparatus as set forth in claim 18, wherein the analog circuit is a test circuit for converting to a digital signal an analog signal issued from another analog circuit arranged on the semiconductor chip.

21. A semiconductor apparatus comprising:
an analog generation circuit;
a first transmission line for transmitting an output voltage of the analog generation circuit to another circuit or element arranged on the same semiconductor chip as the analog circuit; and
a second transmission line for feeding the voltage transmitted to the another circuit or element back to the analog generation circuit,
wherein the analog generation circuit generates the output voltage according to the fed-back voltage.

22. A semiconductor apparatus wherein a variable logic cell and a variable analog cell are provided in a zone on a semiconductor chip other than block formation zones of original function circuits,

the variable logic cell including:

a variable logic circuit having memory elements for outputting a logic output in response to an input according to memory information of the memory elements;

variable wiring means having switching elements for connecting or disconnecting a plurality of signal lines for connection of the variable logic circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means,

the variable analog cell including:
an analog generation circuit;
variable wiring means having switching elements for connecting or disconnecting a plurality of signal lines for connection of the analog generation circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means.

23. A semiconductor apparatus comprising four memory cells to be alternatively selected according to a combination of signals of positive and negative phases, wherein a variable logic cell and a variable analog cell are provided in a zone on a semiconductor

chip other than block formation zones of original function circuits, the variable logic cell including:

a plurality of variable logic cells arranged to outputting signals of positive and negative phases according to memory data of the selected memory cell;

variable wiring means having switching elements for connecting or disconnecting a plurality of signal lines pairs for connection of the variable logic circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means,

the variable analog cell including:

an analog generation circuit;

variable wiring means having switching elements for connecting or disconnecting a plurality of signal lines for connection of the analog generation circuit with at least another variable logic circuit and signal lines mutually intersected; and

wiring-line connection state memory means for storing states of the switching elements of the variable wiring means, and wherein the variable logic cell transmits a signal via the signal lines pairs in a differential system, and the variable analog cell outputs a voltage generated via one of the signal lines in pair and receives a feedback voltage via the other of the signal lines in pair.

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